AD-A031 824 TRANSPORTATION SYSTEMS CENTER CAMBRIDGE MASS F/G 17/7
REQUIREMENTS FOR DABS COMPUTER PERFORMANCE MEASUREMENTS.(U)
SEP 76 J DUMANIAN, D CLAPP

UNCLASSIFIED TSC-FAA-76-21 FAA-RD-76-151 NL

| OF |
AD
A031 824

END

DATE
FILMED
12-76

F.G.

REPORT NO. FAA-RD-76-151

(12)

ADA031824

REQUIREMENTS FOR DABS COMPUTER PERFORMANCE MEASUREMENTS

John Dumanian
David Clapp

U.S. DEPARTMENT OF TRANSPORTATION
Transportation Systems Center
Kendall Square
Cambridge MA 02142

SEPTEMBER 1976

INTERIM REPORT

Prepared for

U.S. DEPARTMENT OF TRANSPORTATION
FEDERAL AVIATION ADMINISTRATION
Systems Research and Development Service
Washington DC 20591

NOTICE

This document is disseminated under the sponsorship of the Department of Transportation in the interest of information exchange. The United States Government assumes no liability for its contents or use thereof.

NOTICE

The United States Government does not endorse products or manufacturers. Trade or manufacturers' names appear herein solely because they are considered essential to the object of this report.

Technical Report Documentation Page

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
FAA-RD-76-151		

4. Title and Subtitle
REQUIREMENTS FOR DABS COMPUTER PERFORMANCE MEASUREMENTS

5. Report Date
September 1976

6. Performing Organization Code

7. Author(s)
John Dumanian
David Clapp

8. Performing Organization Report No.
DOT-TSC-FAA-76-21

9. Performing Organization Name and Address
U.S. Department of Transportation
Transportation Systems Center
Kendall Square
Cambridge MA 02142

10. Work Unit No. (TRAIS)
FA636/R6159T

11. Contract or Grant No.

12. Sponsoring Agency Name and Address
U.S. Department of Transportation
Federal Aviation Administration
Systems Research and Development Service
Washington DC. 20591

13. Type of Report and Period Covered
Interim Report
February — June 1976

14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

Special equipment for measuring the computing power of a complex of computers in the DABS (Discrete Address Beacon System) is described.

17. Key Words	18. Distribution Statement
DABS, Discrete Address Beacon System, Computer Performance Measurements	DOCUMENT IS AVAILABLE TO THE U.S. PUBLIC THROUGH THE NATIONAL TECHNICAL INFORMATION SERVICE, SPRINGFIELD, VIRGINIA 22161

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price
Unclassified	Unclassified	20	

Form DOT F 1700.7 (8-72) Reproduction of completed page authorized

-A- 407082 -B

PREFACE

This document contains the specifications of computer performance measurement equipment to measure the computer power of the DABS (Discrete Address Beacon System) Site Processor. It is a required item of the Project Plan Agreements FA-636 DABS/IPC Site Processor Support Program.

A contract was awarded to Texas Instruments in February 1976 to develop and install 3 DABS Sensor Systems in the Atlantic City and Philadelphia areas. Provisions were not made to test these systems (which are engineering models) for the computer power and memory storage being consumed, and for the efficiency of the software. To specify the computer hardware and software of the production version of the DABS Site Processor, computer performance measurements are necessary. For example, the global memory file lengths, the queuing delays to access global memories, and the times spent in major routines need to be measured.

This document describes the changes necessary to remote the measurement data to a processor-memory, which will collect and reduce the data that will ultimately serve as an information source for producing the specification of the production version of the DABS Computer hardware and software.

METRIC CONVERSION FACTORS

Approximate Conversions to Metric Measures				Approximate Conversions from Metric Measures			
Symbol	When You Know	Multiply by	To Find	Symbol	When You Know	Multiply by	To Find
LENGTH				**LENGTH**			
in	inches	2.5	centimeters	mm	millimeters	0.04	inches
ft	feet	30	centimeters	cm	centimeters	0.4	inches
yd	yards	0.9	meters	m	meters	3.3	feet
mi	miles	1.6	kilometers	m	meters	1.1	yards
				km	kilometers	0.6	miles
AREA				**AREA**			
in²	square inches	6.5	square centimeters	cm²	square centimeters	0.16	square inches
ft²	square feet	0.09	square meters	m²	square meters	1.2	square yards
yd²	square yards	0.8	square meters	km²	square kilometers	0.4	square miles
mi²	square miles	2.6	square kilometers	ha	hectares (10,000 m²)	2.5	acres
	acres	0.4	hectares				
MASS (weight)				**MASS (weight)**			
oz	ounces	28	grams	g	grams	0.035	ounces
lb	pounds	0.45	kilograms	kg	kilograms	2.2	pounds
	short tons (2000 lb)	0.9	tonnes	t	tonnes (1000 kg)	1.1	short tons
VOLUME				**VOLUME**			
tsp	teaspoons	5	milliliters	ml	milliliters	0.03	fluid ounces
tbsp	tablespoons	15	milliliters	ml	milliliters	2.1	pints
fl oz	fluid ounces	30	milliliters	l	liters	1.06	quarts
c	cups	0.24	liters	l	liters	0.26	gallons
pt	pints	0.47	liters	m³	cubic meters	35	cubic feet
qt	quarts	0.95	liters	m³	cubic meters	1.3	cubic yards
gal	gallons	3.8	liters				
ft³	cubic feet	0.03	cubic meters				
yd³	cubic yards	0.76	cubic meters				
TEMPERATURE (exact)				**TEMPERATURE (exact)**			
°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C	Celsius temperature	9/5 (then add 32)	Fahrenheit temperature

CONTENTS

1. INTRODUCTION

To monitor the performance of the multiple computers and memories in the DABS Computer Complex, over 300 sensors are required; this cannot be satisfied by commercial CP Computer Performance measurement equipment. In addition, sensing points are not easily available on the current design of the DABS 990/10 computers. These reasons point to the use of customized CP measurement equipment.

The requirements for such equipment are:

1. A T.I. 990/10 computer (possibly a spare DABS computer) to be used as the Controller, Data Collector, and Data Reducer for the computer performance measurement function during the DAB System operational tests.

2. Three standard T.I. peripherals – the ASR-733 Data Terminal with dual cassetts storage, the DS-31 Disc System, and the 913 VDT Display – to augment the 990/10 Computer.

3. Specially designed cable drivers on the DABS Computer boards and specially designed TILINE I/O boards for the performance-measuring 990/10 computer.

2. MEASUREMENT

2.1 DABS FUNCTIONS TO BE MEASURED

The important functions being processed by the DABS Computers are shown below. The computers which process these functions are those which merit measurement.

1. Channel Management

   Transaction Preparation
   Target List Update
   Roll Call Scheduling
   Transaction Update

2. Surveillance

   Preprocessing
   Correlation
   Tracking

3. Intermittent Positive Control

   Input A, Track A
   Epoch 1
   Epoch 2
   Epoch 3
   Epoch 4
   Conflict Table Exchange

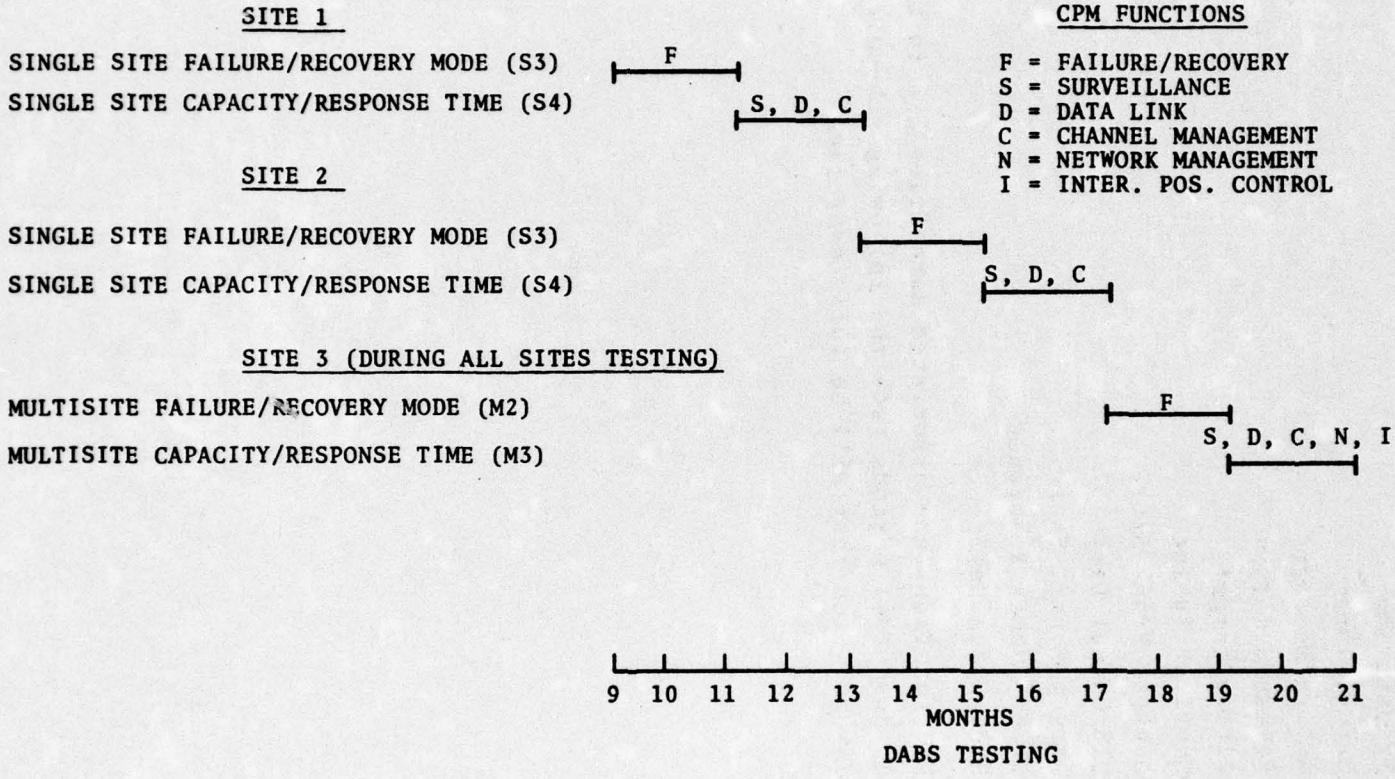
4. Other

   Data Link Processing
   Network Management
   Failure Recovery

2.2 DABS FILE LENGTHS TO BE MEASURED

Transaction
Surveillance
Active Message
Released Target
Active Target
Conflict Tables
Central Track Store
CTS Output List
Target Report Store
ATCRBS Cross Reference
DABS Cross Reference

The functions and associated data files are to be measured during those test periods (see the following schedule of test periods) in which they will be fully exercised.



COMPUTER PERFORMANCE MEASUREMENT TESTING SCHEDULE

3. SYSTEM ARCHITECTURE

3.1 DABS COMPUTER BOARD CHANGES

The DABS memory-voter board shall be examined as a place for installing cable drivers and connectors for remoting the data to the TILINE input of the computer performance measurement computer. Part of this document is a statement of work which describes these changes and the design of special TILINE I/O Interface boards.

3.2 SPECIAL TILINE I/O BOARD

In order to make accurate and precise timing measurements, specially designed TILINE I/O boards for the measurement computer are needed. Four types of boards are described in the statement of work section of this document.

3.3 MEASUREMENT COMPUTER AND PERIPHERALS

The special TILINE I/O boards are to be part of the measurement computer system. They will be plugged into the MC Measurement Computer TILINE. A CRU Communications Register Unit will also be part of the MC system. T.I. interface cards for the DS-31 Disc, 913VDT Display, and ASR-733 Data Terminal will be plugged into the CRU.

The MC will be a dual 990/10 DABS computer, which includes a memory-voter board and two arithmetic unit boards. It is estimated that 3K-words will be used for the data collection and partial reduction program, and 5K-words will be used for buffer storage for disc and display transfers.

4. DATA REDUCTION

4.1 DATA COLLECTION AND PARTIAL REDUCTION

The program times and file length data which are collected in the MC are to be processed, partially reduced, displayed, and stored on disc.

The elapsed time of routines (programs) and the lengths of files are to be determined; from these, averages and standard deviations are to be calculated. Large departures from the average will be noted and preserved. For example, when a sample exceeds 3σ of an average, the magnitude and the time it occurred will be recorded on disc. Averages will be recorded on disc and displayed.

Six sectors (or 864 words) of data will be recorded on disc at one time. New averages will be generated approximately every minute of the test runs, which normally last several hours. The identity of the average, number of samples, and the time will be recorded along with the average. The one minute averaging intervals will be overlapped among the quantities being averaged in order to insure an even flow of information to the disc system. Other parameters such as the numbers of targets shall also be recorded at one minute intervals.

An option exists for eliminating the Display as a real time monitor. The ASR-733 Data Terminal may be used in a time-shared manner. It may print output averages, then allow time periods for operator insertion of control characters (prior to making parametric changes in the data collection and reduction programs). Once the operator seizes control, normal output printing is discontinued; it is resumed when the operator relinquishes control.

4.2 OFF LINE DATA REDUCTION

After a test run, all of the previously recorded data on the disc will be read in and averages and standard deviations for a run will be calculated and printed. Large deviations can also be printed (an operator option).

Average and peak computer power (per computer), maximum and average file lengths, and peak and average queuing delays will be calculated. All these will be printed on the ASR-733.

5. STATEMENT OF WORK

5.1 METHODOLOGY FOR MEASURING DABS COMPUTER PERFORMANCE

A method will be devised for measuring the performance of the computers and memories in the DABS Computer Complex by designing drivers for cabling data from the computers in the Computer Complex to a performance measurement computer, by designing reveivers, comparators, and timers to establish time "stamps" on the collected data, and by outlining the steps for reducing the data in an off-line manner on the 990 performance measurement computer.

These three tasks are described in detail below.

5.2 TASK 1. DRIVERS AND CABLING

Circuity will be designed, and the drivers and cabling which will be required to remote the data necessary to measure the functions specified in Section 6 below will be specified as DABS computer hardware changes. Global memory addresses and contents, local memory addresses, TILINE Bus Mastership recognition, and error and status signals appear to be the data points required; these points may be amended as long as means are available for measuring the functions specified in Section 6 and as long as the computers performing the individual functions are identifiable.

The integrated circuit drivers, cables, connectors, tie points, and physical location of the circuit drivers, connectors, etc., will be specified.

5.3 TASK 2. TILINE INPUT/OUTPUT BOARD

A TILINE Input/Output Board will be designed for installation in the performance-measuring computer to receive data from the DABS Computer Complex and to furnish data time-of-arrival indications. The TILINE Input/Output Boards will be of at most four types, which are described below. These types may be combined. It is expected

that as many as four data input sensors of the same type may be on one board.

5.3.1 Type 1 Global Memory File Length

In global memory there are buffers or files which are accessed by operational computers. Usually there is a register in the global memory that points to the start (or first) address of a file and another that points to last (currently used) address of a file. In order to know the current file length, the contents of these two registers must be sampled (whenever an operating computer is accessing them). Thus the TILINE I/O board will be required to have two sections dedicated to finding the start and current address of a global file. The I/O board does this by receiving from the performance measuring computer 24 global address bits, and by combining 2 bits to signify the section of the board and 2 bits to signify the type of measurement. Two 16-bit words with this information will be supplied by the measurement computer. A buffer register in the I/O board will hold these data (e.g., the memory location, which holds the first address of a file). A comparison circuit will constantly compare the 24 global address bits in the I/O board register wigh global memory (address) requests on the Global TILINES. When a match is made, a 16-bit Global Memory Data word is accepted on the Measurement TILINE I/O board. The most significant 13 bits of the data word and 2 section identity bits are then transferred back to the Measurement Computer. On one I/O board, the lengths of two files can be measured.

The identity of the requesting computer and the time of the request are not needed for this type of measurement.

5.3.2 Type 2 Global Memory Access Times

In a similar manner as in Type 1, the global memory address, section identity, and measurement type bits will be inserted in the I/O board. The type bits will call for a Type 2 measurement. At the moment of insertion, a timer on the I/O board will be started. When an operational computer makes a request of a global memory access which matches the global memory address stored in the I/O

board, a 13 bit time (with the least significant bit = 1.02 microseconds) and 2 section bits will be returned to the measurement computer. This time combined with the Real Time Clock (120 Hz) in the measurement computer will mark the time when a particular operational computer made an access to a particular file.

As many of as four sections can be configured on one I/O board.

5.3.3 Type 3 Program Memory Access Times

In a similar manner as in the previous type, two words can be transferred to the I/O board, which will start the measurement procedure. Actually, only one word is needed since the significant information can be compressed to 16 bits, if a individualized board for this type is designed. Thirteen bits are needed for program memory addresses and three bits for section identity. If this board is restricted for one type of measurement, then no measurement type bits need to be used. Eight measurement sections may be implemented. Thirteen time bits, accurate to 1.02 microseconds, and three section identity bits are to be transferred back to the measurement computer on address matching.

Software routines that have multiple entry and exit address points would require one section per entry or exit.

5.3.4 Type 4 Global Memory Queuing Times

The Type 4 board is a special TILINE I/O board that requires no input initialization. It is to be configured of as many as 16 sections, each of which will output to the measurement computer whenever any global access has been completed or whenever status or error signals are generated. The output word is to be made up of four status bits, one error bit, six queuing time bits, four section bits, and one queuing time indication bit. Whenever any global memory accesses are requested this board will measure the time it takes to grant the access. Six bits of time from .125 microseconds to 8 microseconds will be transferred to the measurement computer with a (Global Memory) queuing time measurement indication bit; error or status signals could accompany these data. A hardware

option should be provided on the board to suppress the status signals. When not suppressed and when the queuing time measurement indication bit is a zero, six bits of time (in the time slot, measuring time from 1.3 milliseconds to 8.2 milliseconds) will be inserted with the status bits. Another hardware option should be provided on the board to permit transfers of only those queuing times in excess of 1 microsecond (all smaller times would not be transferred to the measurement computer).

The global memory queuing time is equivalent to the "time dilation" quantity that is currently being simulated in the Texas Instruments DABS computer model. The quantity referred to is the elapsed time from a read or write request of a Global Memory to the granting of the request to an individual computer in the DABS Computer Complex. The delay times involved include the Local TILINE access time, the coupler-to-coupler connection time, the Global TILINE access time, and the Global Memory access time. The "time dilation" quantity is a function of the individual computer, the number of computers in the computer complex, and the aircraft activity or loading on the computer complex.

6. DABS FUNCTIONS TO BE MEASURED

In order to understand the use of the monitoring points and the timing data, a description of the functions to be measured is shown below.

6.1 CHANNEL MANAGEMENT

During the single site Capacity/Response Time (S4) tests for sites 1 and 2 and the Multisite Capacity/Response Time (S4) tests at site 3 (as described in the Test Plan, MITRE report MTR 6987) the Channel Management function will be measured. The elapsed time from the beginning a DABS period to the start of the first schedule and the elapsed time between schedules will be measured. The elapsed time for ATCRBS periods and the elapsed time for DABS periods will be measured. The elapsed times in Transaction Preparation, Target List Update, Transaction Update, Roll Call Scheduling, and Channel Control will be individually measured. The elapsed times will be time tagged and means for identifying them to particular 4 second intervals should be provided. Also, during the Transaction Preparation measurement, the Transaction Buffer length will be measured.

Included with the Target List Update will be the Active Target List length measurement. Included with the Roll-Call Scheduling measurements will be the measurement of the Transmission Buffer Length.

The majority of the above data will be reduced off-line once a day after the tests are run. Eligible to be shown on a display once every 4 seconds are the total number of aircraft transactions in each of the subroutines except Channel Control, the % computer time in each of the five subroutines, the total DABS time, and the total ATCRBS times.

6.2 SURVEILLANCE

Measurements of activity will be made during surveillance processing by measuring the time spent by the surveillance processor

in each of the subfunctions for both ATCRBS and DABS targets. For ATCRBS, time spent in Input Preprocessing, Target to Track Correlation, Track Initiation, False Target Report/Track Flagging, Radar/Beacon Correlation, ATCRBS Fruit Rejection, and Track Update will be measured. For DABS, Input Preprocessing, Position Measurement Selection, Track Initiation, False Track Rejection, Radar/Beacon Correlation, and DABS Track Update will be the objects of measurement. As the test program develops, it may be necessary to break down these routines into smaller segments for measurement.

For both DABS and ATCRBS processing, the flow of surveillance information in and out will have to be monitored. For this purpose, the time spent in Track Data Message Processing and in Surveillance Data Dissemination will be determined and correlated with numbers of messages processed.

6.3 IPC

The evaluation of computer performance on the IPC task, like that on Surveillance, will require knowledge of the entry points to each of the major routines to start with and to selected lower level routines as the testing proceeds. The sequence of IPC processing is quite complex because of the requirement to do sector processing at a rate different from epoch processing. As a result, the number of different measurements taken during IPC will probably be greater than that for more straightforward functions such as Surveillance.

As a minimum, the elapsed times spent in the Coarse Screen (TPCSN), Resolution (TPMSR), Preparation (TPPWI), Tracker (TPTRK), and Detector (TPDET) routines will be measured.

6.4 OTHERS

The Network Management, Data Link Processing and Failure/Recovery elapsed times will be measured. The delay times (those greater than normal) for the extraction of data from Global memories will also be measured.